ABSTRACT OF THE DISCLOSURE:

A parity generating circuit [[201]] in a 0 side [[20]] receives input signals [[s21]] on respective signal lines and produces a parity bit [[p20]] based on the input signals [[s21]]. A parallel/serial converting circuit [[203]] multiplexes parallel signals [[s22]] (or input signals [[s21]]) and the parity bit [[p20]] into a serial signal [[s23]] with reference to a timing signal [[t20]]. A serial/parallel converting circuit [[211]] in a 1 side ~~21 is~~ reproduces parallel signals [[S24]] and a parity signal [[p21]] and produces a parity check timing signal [[t21]]. A parity checking circuit [[212]] checks a parity of the parallel signals [[s24]] by the use of the parity signal [[p21]]. If normal, a state holding circuit [[213]] holds outputs [[s25]] of the parity checking circuit [[212]] as a state signal. If abnormal, held content of the state holding circuit [[213]] is cleared.